



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,909	11/03/2003	Jason Harold Culler	200310794-1	5350
22879 7590 03/07/2007 HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			EXAMINER RAHMAN, FAHMIDA	
			ART UNIT	PAPER NUMBER
			2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

# Office Action Summary

Application No.

10/699,909

Applicant(s)

CULLER, JASON HAROLD

Examiner

Fahmida Rahman

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 07 December 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-15, 18 and 20-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15, 18 and 20-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This action is in response to communications filed on 12/07/2006.
2. Claims 1, 15, 25, 30 32, 34 have been amended, claim 38 has been added and claims 16-17, 19 have been cancelled. Thus, claims 1-15, 18, 20-38 are pending.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 25, 26, 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Bi et al (US Patent Application Publication 2003/0052662)

For claim 1, Bi et al teach the following limitations:

**A system comprising:**

**a sample network (Fig 4) that provides plural samples (211, 221) of an input signal state (201) associated with different time instances of the input signal (230 samples 201 at time t-T, 211 correspond to t, 221 corresponds to t+T), each of the plural samples corresponding to the input signal delayed by a known amount of time (201 correspond to t-T, 221 correspond to t+ T, 211 corresponds to t. Therefore,**

Art Unit: 2116

these samples represent input signal delayed by known amount of time); **and a detector (290) that determines the frequency for the input signal ([0040]) based on samples of the input signal state for different time instances of the input signal residing within one period of the input signal** (the input samples at  $t$ ,  $t-T$ ,  $t+T$  resides within one period of  $y_t$ . [0010] discussed the background work that refers Ishikawa (US Pat 5444416). Ishikawa shows details of how samples are collected. Fig 3 shows that these samples are collected over one period of  $y_t$ ), **and the known amount of time for each of the plural samples** ( $T$  is the known amount of delay that is used in equation as shown in [0023]), **the detector provides a value that represents the frequency of the input signal ([0040])**.

For claims 25 and 30, Bi et al teach the following limitations:

**A frequency detection system comprising:**

**means for sampling (Fig 4) an input signal (201) having an unknown frequency** (the system determines the frequency of the FM modulated signals as explained in abstract) **and for providing plural indications of signal state** ( $y_t$ ,  $y_{t-T}$ ,  $y_{t+T}$  as shown in [0021]) **associated with different time instances of the input signal delayed for different amounts of time** (210 delays 201 to produce  $y_t$ , 220 delays 211 to produce  $y_{t+T}$ . Therefore, 230 receives two inputs: 221, which represents  $y_{t+T}$ , a delayed signal by  $2T$  as shown in Fig 4, and 221, which represents  $y_{t-T}$ , undelayed signal. 240 receives 211, which represents  $y_t$ , a delayed signal by  $T$  as shown in Fig 4. Therefore, signals different time instances of input signals are delayed by different amounts of

Art Unit: 2116

time); and means for determining a frequency for the input signal ([0021]) based on the plural indications of signal state that correspond to time instances of the input signal residing within a single period of the input signal and the known amount of time (the input samples at  $t$ ,  $t-T$ ,  $t+T$  resides within one period of  $y_t$ . [0010] discussed the background work that refers Ishikawa (US Pat 5444416). Ishikawa shows details of how samples are collected. Fig 3 of Ishikawa shows that these samples are collected over one period of  $y_t$ . Frequency determination depends on collecting samples delayed by the known amounts of time); and means for providing a corresponding of frequency value for the determined frequency (Fig 4).

For claim 26, delaying means are selected parts of sampling means.

4. Claim 15 is ejected under 35 U.S.C. 102(e) as being anticipated by Majos (US Patent 6701445).

A system comprising:

a plurality of storage elements (14, 15, 16, 17 of Fig 2), the plurality of storage elements being clocked to latch (Fig 2) different time instances of an input signal (1H in Fig 2) to provide corresponding output samples of the input signal ( $Q_1(T_n)$ ,  $Q_2(T_n-k)$ ,  $Q_3(T_n+dt)$ ,  $Q_4(T_n-k+dt)$  of Fig 2) sufficient for determining a frequency value ( $H^+$ ,  $H^-$ ) of the input signal (3 determines frequency value  $H^+$ ,  $H^-$  from  $Q_1$ - $Q_4$ );

Art Unit: 2116

a plurality of delay elements (11, 12) associated with at least a substantial number of the storage elements (11-12 are associated with 14-17, each of the delay elements delaying a sample signal (1E) by a respective known amount of time (R1 is defined and dt is predetermined; lines 20-45 of column 5) to provide a respective clock signal (Fig 2) that clocks a respective one of the at least a substantial number of the storage elements (clock signals clock 14-17 in Fig 2) to latch a respective one of the different time instances of the input signal (the different instances of input signal is latched as shown in Fig 2) to provide at least a portion of the corresponding output samples (Fig 2); and a detector (3) that provides a frequency value (H+, H-) for the input signal (combination of H+, H- is a frequency value for the input signal as the combination provides indication of frequency of H as explained in table of column 7) based (i) on output samples that correspond to different time instances of the input signal (Q1-Q4 are input to 3 as shown in Fig 1) and (ii) the known amount of time for each respective delay element (samples are dependent on the R1 and dt time. If R1 is not chosen properly, the width of clock signal can be zero and the samples may not be produced. Q3 and Q4 are directly related dt as shown in Fig 2. As samples are based on R1 and dt and 3 provides frequency value based on samples, the detector provides frequency value based on output samples and the known amount of time).

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2116

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2-9, 11, 27, 28, 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662), in view of Lee et al (US Patent 6326826).

For claims 2-3, 31-33, Bi et al do not teach plurality of storage elements. Lee et al teach plural storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF\_CK at the output of delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bi et al and Lee et al. One ordinary skill would be motivated to use storage elements with delay elements when sequential design is preferred.

For claim 4, input signal REF\_CK is delayed by delay elements.

Art Unit: 2116

For claims 5 and 6, clock signal activates the storage elements in Fig 2 of Lee. However, neither Bi nor Lee teaches that the oscillator generates the clock signal that is activating the storage.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal REF\_CK, since oscillator provides an on-chip generation of clock signal. The oscillator generated signal is divided by PLL and therefore, oscillator generated clock typically has higher frequency than the supplied clock.

For claims 7, Lee et al teach 7 storage elements (22') to provide samples (EDGE[N]) corresponding to plural samples of REF\_CK at the output of 7 delay elements. The system of Lee et al further comprises delay elements (Delay0-Delay6) with fixed known amount of delay for delayed clock signal (CK[N]) to clock storage 22' to sample input signal at different time interval (the plural samples of input signal just at the end of delay elements are sampled at different time interval) and thereby providing plural samples of the input signal state to the decision logic 23.

For claim 8, delay components are in series. The oscillator can be used to generate a clock from which REF\_CK can be generated.

For claim 9, note Fig 1.



For claim 11, Lee provides the plural storage to latch samples concurrently (i.e., within one period) to the detector.

For claims 27 and 28, Bi et al do not teach any clock signal. Lee teaches delaying clock signal (Fig 1) to provide activation signal to control sampling and plural means of storing signal (Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bi et al and Lee et al. One ordinary skill would be motivated to use storage elements with delay elements when sequential design is preferred.

For claims 34 and 35, Lee et al provides clock to control activation and delays propagation of signal through the plural storage elements having known amount of delay to establish the time intervals (Fig 1 and Fig 2).

6. Claims 10 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662), further in view of Lee et al (US Patent 6326826), further in view of Majos (US Patent 6701445).

Art Unit: 2116

For claims 10 and 29, neither Bi et al nor Lee et al teach that the input signal is directly connected to storage. Majos teaches that the input H is directly connected to the plurality of storage. One ordinary skill would be motivated to connect the input directly to the plural storage as that would provide a faster design.

7. Claims 12, 13, 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662), in view of in view of Majos (US Patent 6701445).

For claims 12, 13, 36 and 37, Bi et al do teach any comparator. Majos teaches a comparator (3) that provides comparison signal (H+ and H-) based comparing desired value (frequency of Din) and actual value (frequency of H). 4 and 5 are the controller that adjusts the clock signal based on comparator signal.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Bi et al and Majos. One ordinary skill would be motivated to adjust the clock signal to get synchronized with data.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bi et al (US Patent Application Publication 2003/0052662).

Art Unit: 2116

Bi et al do not explicitly mention about IC chip. Examiner takes an official notice that the system implemented within the IC chip is well known in the art. An ordinary skill in the art would have been motivated to implement the system within the IC chip for many reasons, such as, to make commercially available to the customers. Bi et al addressed the practicability for implementation in hardware ([0013]). Therefore, the system can be adapted to an IC chip.

9. Claims 18, 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445), in view of Lee et al (US Patent 6326826).

For claim 18, Majos teaches the plurality of delay elements (R1, dt) to provide the respective delayed clock signals (clock to 14-15 has 0 delay, clock to 16-17 has dt delay) for clocking the at least a substantial number of the storage elements to latch the different time instances of the input signal into the storage elements (Fig 2). Majos does not teach that the input signal comprises the sample signal and the input signal being delayed by the plurality of delay elements.

Lee et al teach input signal comprises sample signal, the input signal delayed by delay elements (Fig 1).

Art Unit: 2116

It would have been obvious for one ordinary skill in the art to combine the teachings of Majos and Lee. One ordinary skill would be motivated to have the input signal comprises the delay signal depending on his design criterion.

For claim 21, Lee et al teach that the delay elements (18') provide respective clock edges (CK[1:7] in Fig 2) for activating the storage elements (22'), each of the clock edges corresponding to a different delayed version of the clock signal (11).

For claim 22, the delay elements in 11 of Lee et al are connected in series.

For claim 23, Majos teaches that the input H is directly connected to the plurality of storage.

For claim 24, 14-15 of Majos are clocked at an interval "0" and 16-17 are clocked at interval "dt" to latch the output samples to the detector concurrently.

10. Claims 20 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos (US Patent 6701445).

For claim 20, lines 60-62 of Majos mention that sample signal is a clock signal. However, it does not mention oscillator.

Art Unit: 2116

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal, since oscillator provides an on-chip generation of clock signal.

For claim 38,  $H^+$  and  $H^-$  are not expressed in unit of inverse of period. However, system of Majos provides corrected frequency  $H_{out}$  from  $H^+$  and  $H^-$ , which is in unit of inverse of a period of the input signal.

### **Response to Arguments**

Applicant's arguments with respect to claim 1-15, 18, 20-38 have been considered but are moot in view of the new ground(s) of rejection.

### **Conclusion**


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent

Art Unit: 2116

Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman  
Examiner  
Art Unit 2116



**THUAN N. DU**  
**PRIMARY EXAMINER**